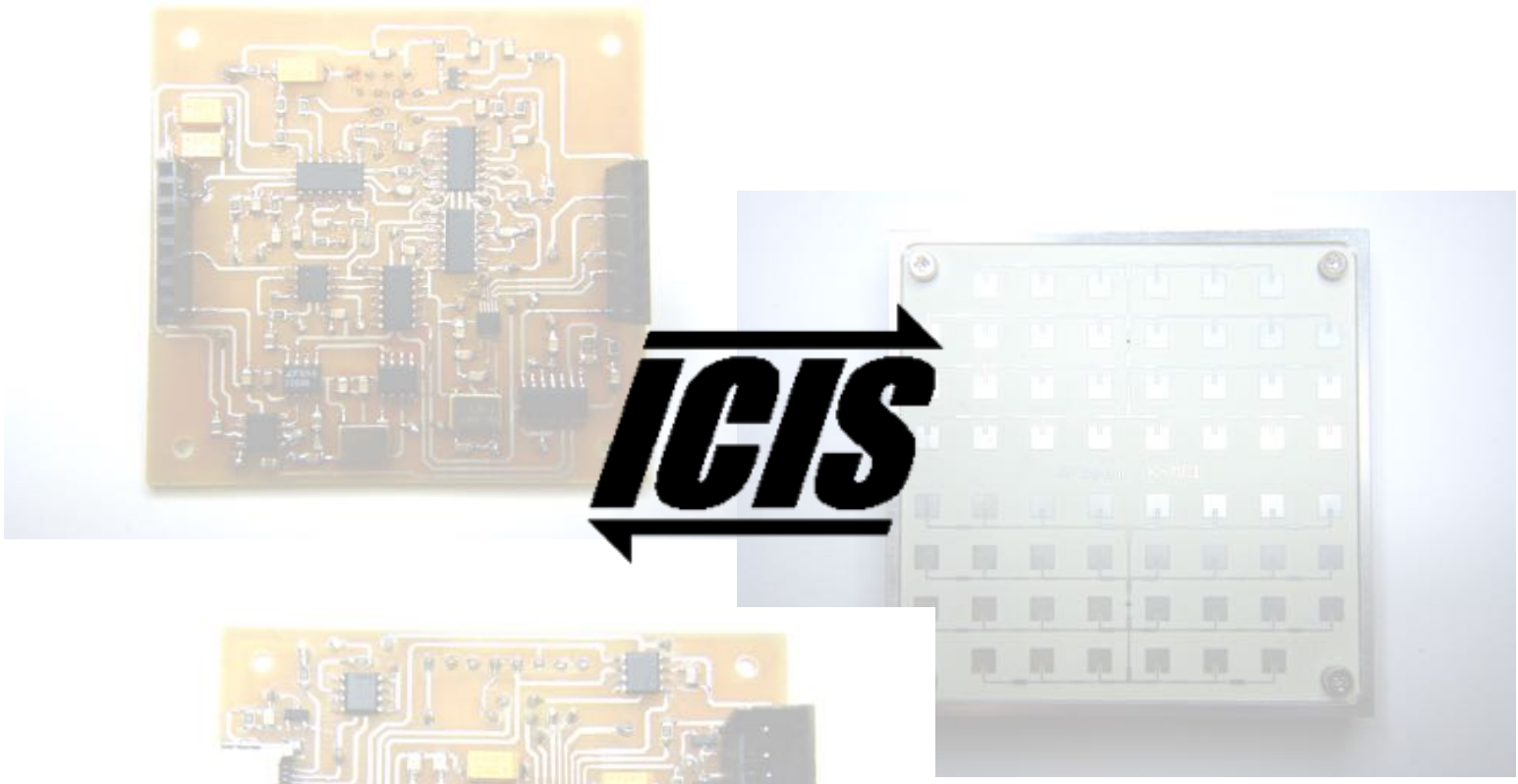

Automotive Collision Mitigation System

Imminent Collision Intervention Systems

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INSTITUTE OF TECHNOLOGY and ADVANCED LEARNING

Electronics Engineering Technology (Telecommunications) & Computer Engineering Technology

TECHNOLOGY PROJECT

FINAL REPORT

Imminent Collision Intervention Systems

Document Title	**Final Report for Automotive Collision Mitigation System**				
Document Number	FR-R1			**Revision**	NEW
Date Issued	2009-04-23	**Date Effective**		**Replaces**	NA

Reviewer(s)

	Name	Title	Signature	Date
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REVISION HISTORY

Revision	Description of Change	Effective Date
NEW	Initial release of Final Report	2008-12-04

Automotive Collision Mitigation System

1.0 PURPOSE

The purpose of this document is to outline the progress of the Automotive Collision Mitigation System.

2.0 SCOPE

This document is intended to satisfy in part, the requirements of the Technology Project for Terms 5.

This Progress Report is an end of term report that outlines the progress of the Automotive Collision Mitigation System and the current state of the Automotive Collision Mitigation System as of December 4, 2008.

3.0 EXECUTIVE SUMMARY

The purpose of this project is to design an affordable aftermarket microwave radar-based Collision Mitigation System that will alert the driver of an impending collision with another motor vehicle.

The hardware design is complete. The baseband oscillator, USB microcontroller and differential amplifier have been constructed and tested. The USB firmware framework is complete. The basic graphical user interface on the Windows software application has been created, and the USB communication with the microcontroller is operational.

The project is currently behind schedule according to the initial project timeline. However, it is believed that the original timeline was too aggressive and the goals set out could not be achieved based on the allocated time.

The overall project expenditures are currently within the total budget of $1000.

4.0 PROJECT CONCEPT

The system design, operation, and performance will no longer comply with ISO standard 15623:2002 [5] and SAE standard J2400 [6] for forward vehicle collision warning system performance, test procedures, and human interface requirements as specified in the project concept proposal objectives.

5.0 PROJECT REQUIREMENTS

The system will no longer comply with the ISO standard ISO 15623:2002 [5] for motor vehicle forward collision warning system performance and test procedures and SAE standard J2400 [6] for motor vehicle forward collision warning system operating characteristics and human interface requirements as specified in the project requirements document.

6.0 PROJECT PLAN

6.1 Gantt Chart

6.2 Critical Problems

No critical problems have been encountered to date.

6.3 Budget

Figure 1 – Project Budget

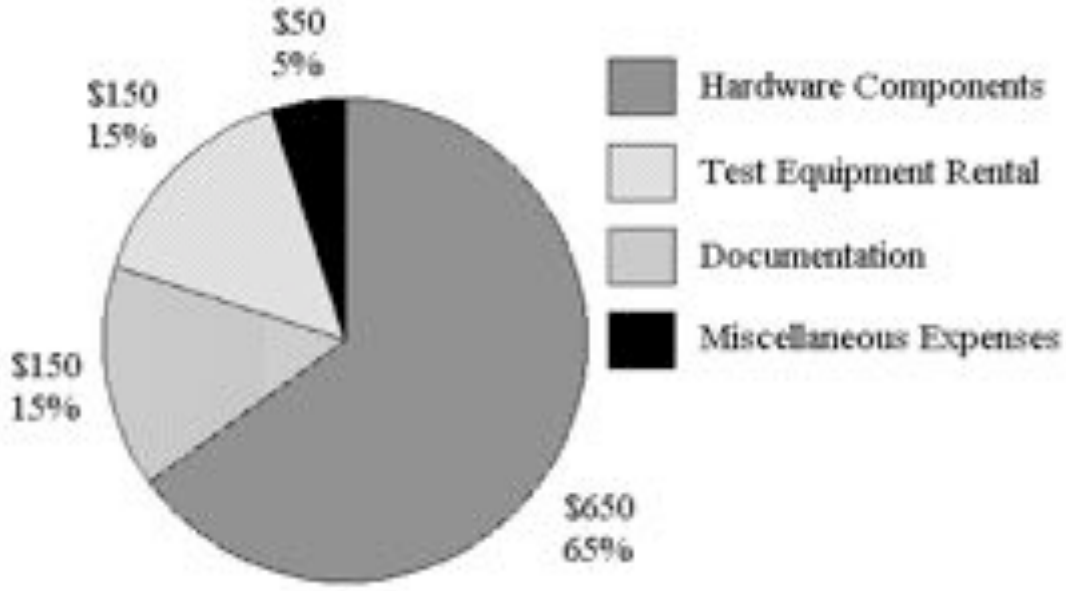


Table 1 – Hardware Components Acquired as of December 4, 2008

Part	Part Number	Quantity	Unit Price
Microwave Radar Transceiver	K-MC1	2	$175.73
8-bit USB Microcontroller	PIC18F2550	2	$4.34
P-Channel MOSFET	MMSF3P02HDR2G	4	$1.41
Direct Digital Synthesizer	AD9833BRMZ	2	$9.90
Transient Voltage Suppressor	NUP4201DR2G	4	$1.46
Level Translator	TXB0104DR	4	$1.52
Red LED	TLMS2100-GS08	3	$0.46
Green LED	TLMG2100-GS08	3	$0.61
100kΩ ⅛W Resistor	MCR10EZPF1003	20	$0.05
330Ω ⅛W Resistor	MCR10EZPF3300	10	$0.05
10kΩ ⅛W Resistor	MCR10EZPF1002	40	$0.05
124Ω ⅛W Resistor	MCR10EZPF1240	10	$0.05
120Ω ⅛W Resistor	MCR10EZPF1200	10	$0.05
200Ω ⅛W Resistor	MCR10EZPF2000	10	$0.05
360Ω ⅛W Resistor	MCR10EZPF3600	10	$0.05
3A 40V Schottky Diode	MBRS340T3G	10	$0.43

0.01µF 50V Ceramic Capacitor	08055C103KAT2A	30	$0.07
0.1µF 50V Ceramic Capacitor	08055C104KAT2A	70	$0.10
48.000 MHz Oscillator	KC7050C48.0000C50D00	2	$3.31
10µF 16V Tantalum Capacitor	TAJC106K016R	8	$0.53
Connector (Right Angle 6 Position)	PPTC061LGBN-RC	2	$0.81
Connector (Right Angle 8 Position)	PPTC081LGBN-RC	2	$0.91
470pF 50V Ceramic Capacitor	0805YC474KAT2A	10	$0.36
Header (Straight 6 Position)	PBC06SABN	4	$1.30
Header (Right Angle 6 Position)	PBC06SBCN	4	$2.11
Header (Straight 8 Position)	PBC08SABN	2	$1.41
Header (Right Angle 8 Position)	PBC08SBCN	2	$2.27
10.000 MHz Oscillator	ASV-10.000MHZ-EJ-T	2	$3.43
1.8432 MHz Oscillator	ASV-1.8432MHZ-EJ-T	2	$3.43
Digital Potentiometer (10kΩ)	MCP4251-103-E/SL	8	$1.66
Operational Amplifier	MCP6244-E/SL	8	$0.97
Digital Signal Controller	dsPIC33FJ256GP710-I/PF	2	$16.30
Operational Amplifier	OP777ARZ	2	$3.01
NPN Transistor	BC846BLT1G	10	$0.17
0.001µF 50V Ceramic Capacitor	08055C102KAT2A	10	$0.08
10µF 16V Tantalum Capacitor	TPSC106K016R0500	4	$0.86
Header (Straight 14 Position)	PBC14SABN	2	$1.81
Header (Straight 24 Position)	PBC24SABN	2	$2.38
Connector (Right Angle 14 Position)	PPTC141LGBN-RC	2	$1.27
Connector (Right Angle 24 Position)	PPTC241LGBN-RC	2	$2.10
Connector (Right Angle 6 Position)	PPTC061LGBN-RC	1	$0.85
15kΩ ⅛W Resistor	MCR10EZPF1502	10	$0.04
33kΩ ⅛W Resistor	MCR10EZPF3302	10	$0.04
39kΩ ⅛W Resistor	MCR10EZPF3902	10	$0.04
200mA 30V Schottky Diode	BAT54LT1G	10	$0.19
256kB Serial EEPROM	25LC256-I/SN	2	$2.76
8th Order Low-Pass Filter	LTC1069-6CS8#PBF	2	$12.15
Instrumentation Amplifier	INA132U	2	$4.38
High Speed JK Flip-Flop	SY100EL35ZG	2	$4.49
220µF 6.3V Tantalum Capacitor	TAJC227K006R	4	$2.72
1MΩ ⅛W Resistor	MCR10EZPF1004	10	$0.05
1kΩ ⅛W Resistor	MCR10EZPF1001	10	$0.05
4.7kΩ ⅛W Resistor	MCR10EZPF4701	10	$0.05
Dual TVS Diode	MMBZ6V2ALT1G	6	$0.38
3.3V 500mA Linear Regulator	LM2937ES-3.3/NOPB	2	$3.09

5.0V 500mA Linear Regulator	LM2937ES-5.0/NOPB	2	$3.09
1.600 MHz Oscillator	CPPFX-X7-A7BCNP	2	$11.29
Total			$654.06

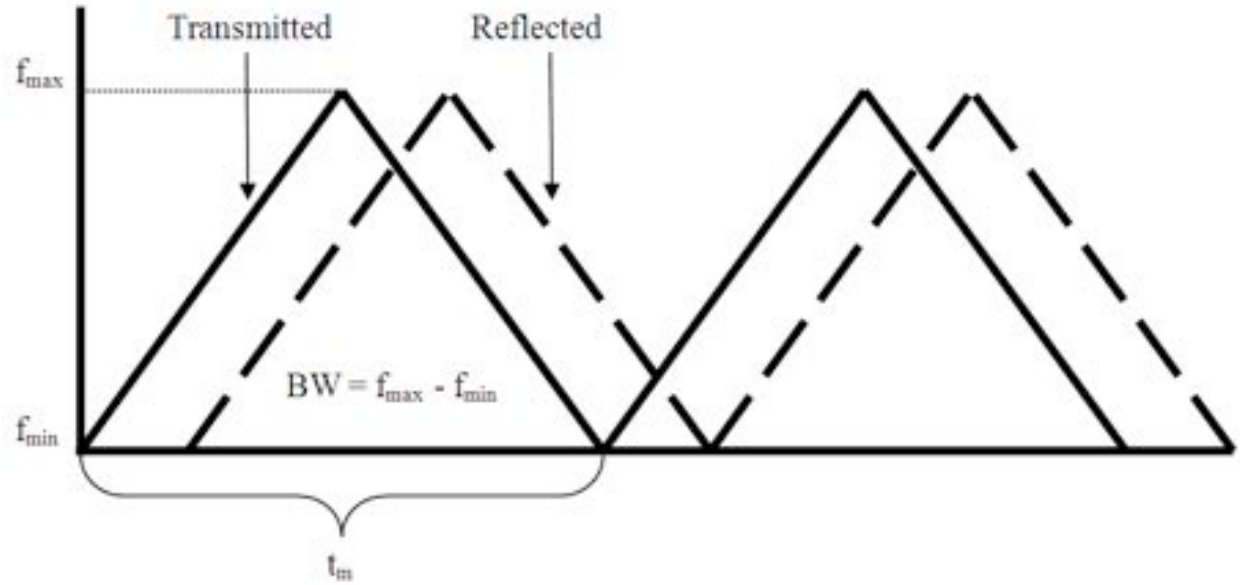
The total project expenditures to date are $654.06, all of it being hardware purchases. The original project budget division allocated $650 to the hardware expenses, which the total hardware purchases exceed. This is not a critical problem since a quantity of the money allocated to test equipment rental, documentation and miscellaneous expenses will be reallocated to the hardware components expenses. The equipment rental expenses, documentation expenses and miscellaneous expenses are not as large as expected. The overall project is expected to stay well within the total budget of $1000.

7.0 HARDWARE PROGRESS

Radar Transceiver

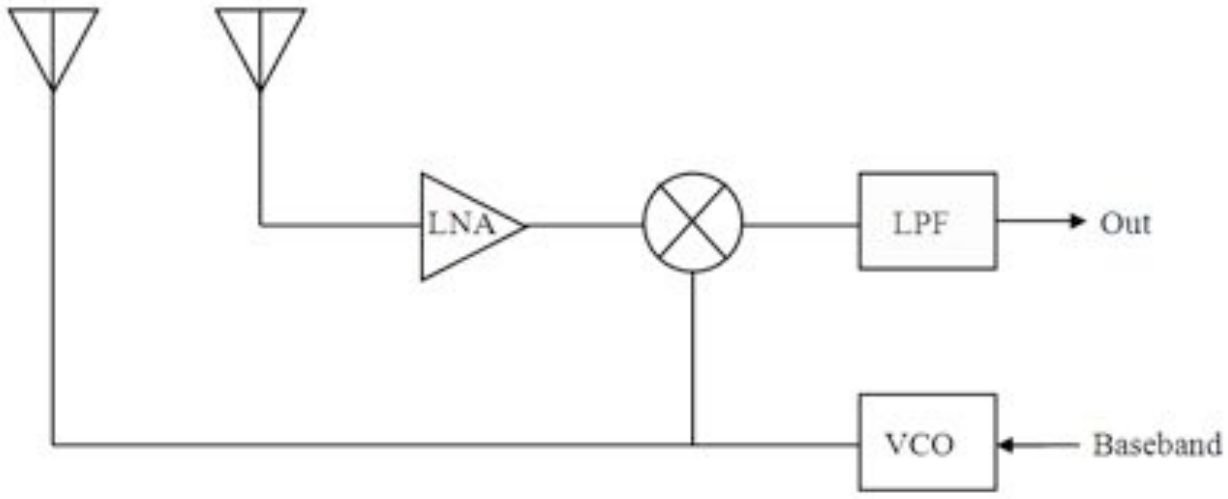
The radar transceiver was ordered on August 19, 2008, from RFbeam Microwave GmbH. To aid in explaining the hardware progress to date, a brief overview of frequency modulated continuous wave is provided in the following paragraphs.

Figure 2 – Frequency Modulated Continuous Wave Transmitted and Reflected Signals



In a frequency modulated continuous wave radar system, the transmitted wave is swept linearly between frequencies f_{min} and f_{max}, and transmitted toward a target. The transmitted wave has constant amplitude but a linear variation with time. At any instant of time the reflected signal is at a different frequency from the transmitted signal by an amount related to the range to the target and frequency of deviation (ramp frequency). As seen in Figure 2, the reflected signal represents a replica of the transmitted signal delayed by the two-way propagation delay time; however, the reflected signal is at a different frequency from that of the transmitter, because the transmitter has moved in frequency during the time the signal propagated from the transmitter to the target and back to the receiver.

Figure 3 – Simplified Radar Transceiver Block Diagram



A FMCW transceiver incorporates a homodyne technique to obtain the range to the target. A sample of the transmitter frequency from the FM sweep oscillator is supplied as the local oscillator to a mixer, and mixed with the reflected signal from the target.

This process gives rise to a differential frequency at the output of the mixer that contains the relevant target information.

Initial testing of the radar transceiver was performed on October 16, 2008. Subsequent tests were performed throughout November using varying target distances from 10 m to 20 m. Using estimates for bandwidth usage, target distances have been determined with accuracies of less than a metre. An example quadrature output signal and associated frequency spectrum for a single target at 20 m are shown in Figures 4 and 5, respectively.

Figure 4 – Quadrature Output Signal (20 m Target Distance)

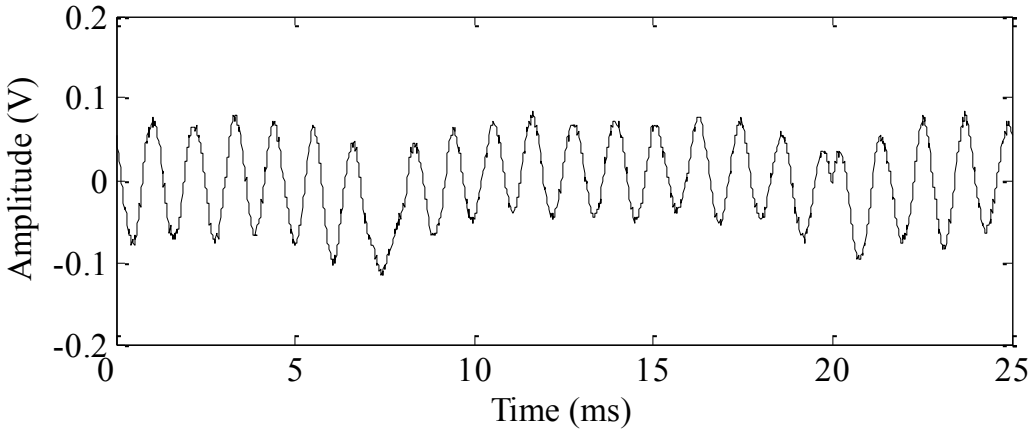
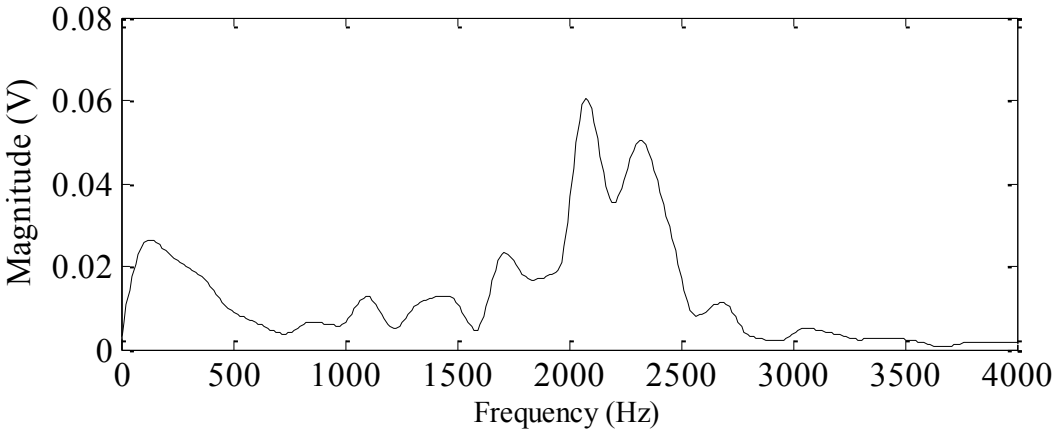


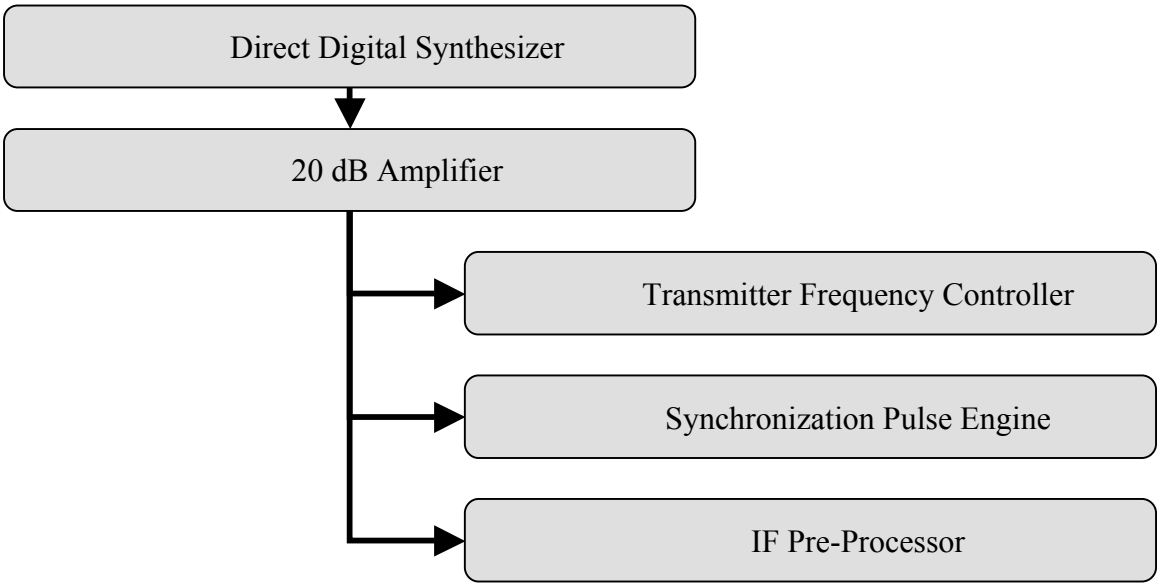
Figure 5 – Frequency Spectrum of Quadrature Output Signal (20 m Target Distance)



$$\text{Range} = \frac{c}{2} \cdot \frac{T_m}{2} \cdot \frac{\Delta f}{BW} = \frac{3.0 \times 10^8 \frac{m}{s}}{2} \cdot \frac{0.01 s}{2} \cdot \frac{2074 Hz}{8.0 \times 10^8 Hz} = 20.6 m$$

Baseband Oscillator

Figure 6 – Baseband Oscillator Block Diagram



The direct digital synthesizer is a software programmable waveform generator. An internal ROM table is created during the initialization sequence that corresponds to the desired output signal shape. A phase accumulator then cycles through the ROM table at a rate determined by the.

Initialization commands were successfully transmitted to the DDS to output a 100 Hz triangular wave.

The DDS output is fed into a 12 dB non-inverting amplifier. The amplified DDS output branches off into three separate circuits for further processing: the transmitter frequency controller, the synchronization pulse engine, and the IF pre-processor.

Transmitter Frequency Controller

The transmitter frequency controller controls the peak-to-peak amplitude and DC offset of the baseband sweep.

The digital signal processor monitors the baseband sweep through an analog channel. If either the peak-to-peak amplitude or DC offset changes such that the transmitter will sweep outside of the prescribed frequency band, the radar transceiver will be immediately disabled.

Synchronization Pulse Engine

The synchronization pulse engine generates a square wave whose positive and negative edges correspond to the slope transitions of the baseband sweep.

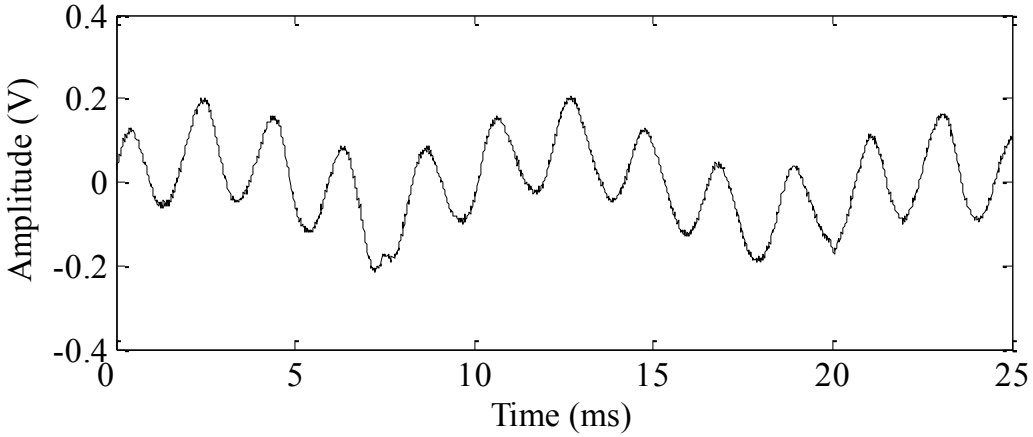
A baseband reference signal is first fed into an active differentiator. The differentiator outputs a DC level relative to the slope of the input.

The output of the differentiator is then fed to a comparator which effectively drives the operational amplifier rail-to-rail upon each transition of the baseband sweep. The signal is then input to the digital signal processor to synchronize the radar output signal sampling interval.

The IF Pre-Processor

The IF pre-processor conditions the radar transceiver IF quadrature output signal prior to filtering. An example radar output waveform for a single target at 10 m distance is shown in Figure 7.

Figure 7 – Quadrature Output Signal (10 m Target Distance)



The differential frequency is the high frequency sinusoidal signal that is used to extract the range of the target. The low frequency triangular wave shape is called carrier feed-through, and is a product of the finite isolation between the transmitter and receiver stages. This triangular

waveform is undesired, and must be removed prior to filtering or sampling of the signal. This task is performed by the IF pre-processor.

The IF quadrature output is first passed through a RC high-pass filter to remove the DC offset from the signal. The signal is then fed to a 20 dB inverting amplifier, and a controlled DC bias of 1.65V is added to the output.

The amplified signal is then fed into the non-inverting input of a differential amplifier. An amplitude matched reference signal from the baseband oscillator is fed to the inverting input of the differential amplifier, effectively subtracting the carrier feed-though from the quadrature output, leaving only the sinusoidal differential frequency.

Initial development of the differential amplifier incorporated an AD820AN general purpose operational amplifier and discrete biasing resistors; however, this circuit will be replaced with a Texas Instruments INA145U instrumentation amplifier that contains integrated precision resistors.

Anti-Aliasing Filter

To prevent aliasing during the sampling process, the quadrature output is passed through an 8^{th} order switched capacitor low-pass filter. The filter cut-off frequency is an integer fraction of the master clock frequency, and is determined as follows:

To achieve the desired cut-off frequency of 32 kHz, twice the maximum input frequency, a master clock frequency of 800 kHz is required. This frequency is generated by a programmable oscillator pre-programmed by the supplier for 1.600 MHz, and then divided by two using a high-speed JK flip-flop.

8.0 SOFTWARE PROGRESS

The Diagnostic Interface is a Windows-based software program that communicates with the Collision Mitigation System via USB.

In the main window of the Diagnostic Interface, there are three menu options; File, Options and Help. In the File menu, there are options to exit the program or open a .hex file. In the options menu, the ‘Baseband Oscillator’ dialog box can be opened. In the help menu, the ‘About Diagnostic Interface’ dialog box can be opened. A flowchart located in Appendix X that illustrates the flow of the software program.

The ‘Baseband Oscillator’ dialog box is capable of sending a value between 0 to FF to the microcontroller to set frequency, set amplitude and set DC offset. It has the options to reset the DSP and Transceiver. The data sent has been verified using MPLAB to read the values from the microcontroller.

The ‘About Diagnostic Interface’ dialog box contains information about the software, such as the software authors and version.

In the main window there are currently 4 buttons; *BURN*, *WRITE*, *READ* and *START*.

The software will be capable of uploading an executable file to the digital signal processor. Selecting the *File – Open* menu option displays the standard Windows "File Open" dialog. Once a file is selected with the .hex extension, the *BURN* button is enabled.

The *BURN* button starts a (partially completed) thread that currently performs the following:

1. Opens the .hex file
2. Translates the data from ASCII to binary
3. Rearranges the data into a more logical form (The Microchip 33F-series INHX32 format is extremely confusing)
4. Stores the data into a dynamically allocated queue

Once the entire file has been successfully translated, it will begin transmitting 64-byte data blocks to the microcontroller. The microcontroller will then relay the data to the DSP via serial peripheral interface (SPI), where a bootloader will perform the flash re-programming sequence.

The *BURN* button is complemented by a progress bar which incrementally increases as each stage of the flash programming sequence is performed.

The *WRITE* and *READ* buttons are only there for testing and will be removed from the final version of the diagnostic interface software. The *WRITE* button is used to send a hex value to the microcontroller by the user entering a value into the adjacent edit control box. The *READ* button reads a hex value from the microcontroller. Once the user hits the *READ* button, the adjacent edit box will display the hex value.

The *START* button is an element of the graphical user interface for the target's distance and velocity. The *START* button will enable the software to read the target's velocity and distance in real-time. Currently the target's velocity and distance is displayed in large font in two edit boxes and shown graphically by the use of two progress bars which move either up or down corresponding to the value of the target's distance or velocity. The distance and velocity is presently simulated by a random number generator. It was added to model how the values of the target's distance and velocity will be shown numerically and graphically.

At the bottom left corner of the main window, there is a status window which displays whether the USB transceiver is connected or not connected. Once a (HID-Class) device with our assigned VID and PID is connected, a thread is then started that waits for commands to send or receive data.

A block diagram illustrating the progress on the Diagnostic Interface can be located in Appendix 3. Also, there is a flowchart located in Appendix 4 that models how the software is being developed.

USB Microcontroller Firmware

The USB firmware framework is complete. The device enumerates successfully, and feature, control, and interrupt reports have been successfully transmitted and received between the host operating system and the microcontroller.

A USB compliant device must have an associated VID (Vendor ID) and PID (Product ID). These two 16-bit values are used by the host operating system to identify a device.

On August 6th an application was granted by Microchip Technology, Inc. to sub-licence their VID and an assigned PID. The approval letter is included in Appendix 6.

USB compliance testing is tentatively scheduled for March, 2009.

Project specific source code has yet to be implemented on the device. However, data has been successfully transmitted to and from the digital signal processor using 8-bit SPI. Minimal development time will be required to complete this stage of the system. Complete integration of the serial communication channel will occur once the digital signal processor is capable of transmitting valid data.

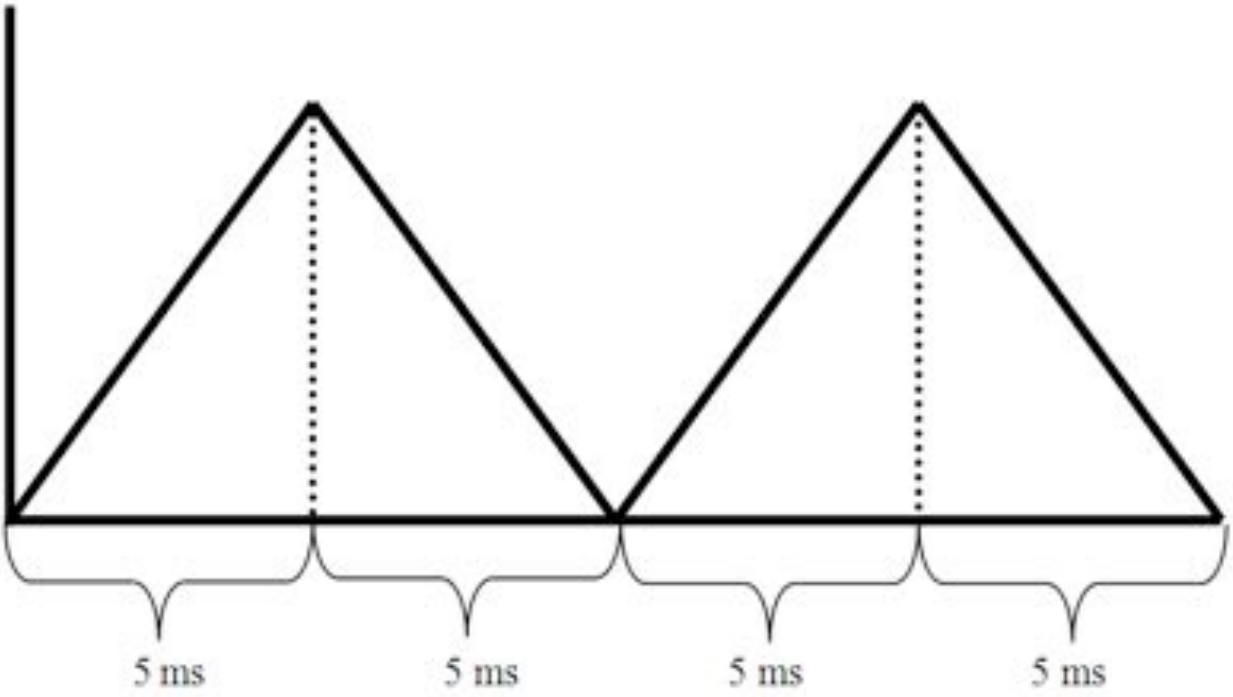
Digital Signal Processor Firmware

The dsPIC33FJ256GP710 digital signal processor incorporates an experimental flash program memory, and as a result has a very limited erase/write cycle count. In addition, the device comes in a 100-TQFP package, which makes replacement of the device difficult. Due to these constraints, initial DSP firmware was developed using a dsPIC33FJ12GP202. Because these two devices utilize identical cores, non-peripheral specific firmware can be developed and tested using the dsPIC33FJ12GP2102 prior to transfer to the dsPIC33FJ256GP710. This reduces the number of flash program memory writes required during firmware development.

The DSP firmware completed to date is a collection of small blocks of code dedicated to initializing the direct digital synthesizer and digital potentiometer via 16-bit SPI.

The following paragraphs give a brief overview of the digital signal processing theory that will be implemented over the coming months.

Figure 8 – Reflected Signal Sampling Window



As shown in Figure 8, the reflected signal from a target is only valid in 5 ms blocks. At every transition of the transmitter sweep, the quadrature output from the radar transceiver will shift 90° in phase and, if the target is not stationary, the differential frequency will also shift.

The synchronization pulse generated from the baseband oscillator will be used to signal the start of a sampling window. However, the reflected signal will be delayed by a time t_d with respect to the synchronization pulse edge. This will introduce frequency measurement errors if the sampling interval begins before the reflected signal has crossed the transition point. While this time delay will be very small for distances less than 150 m, it cannot be ignored.

Figure 9 – Delayed Slope Transition Point

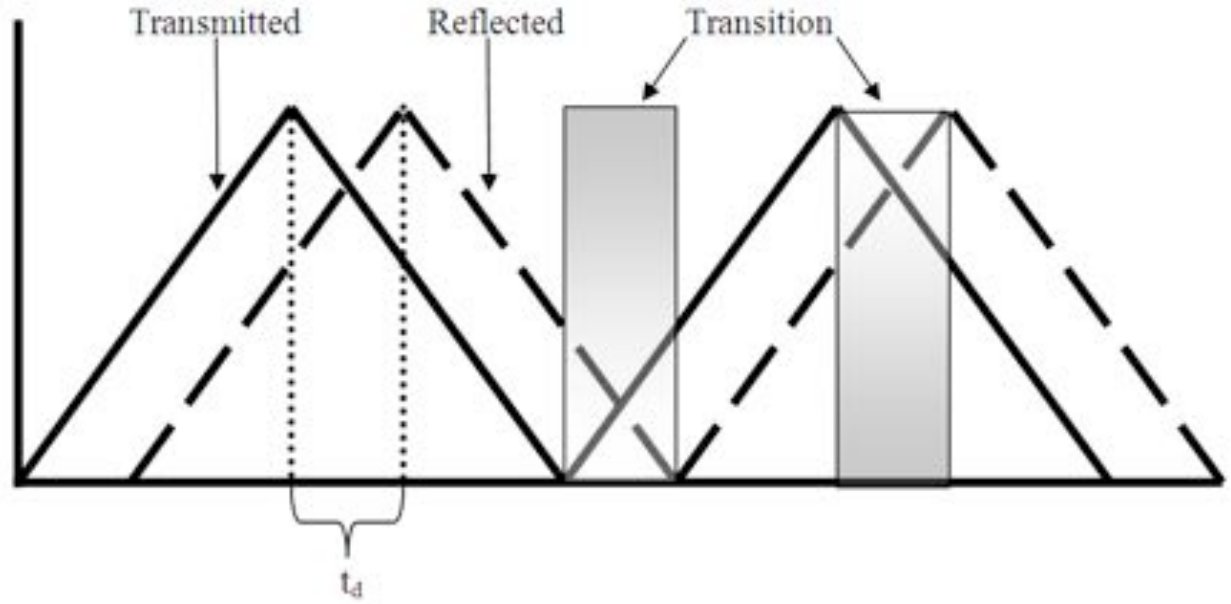
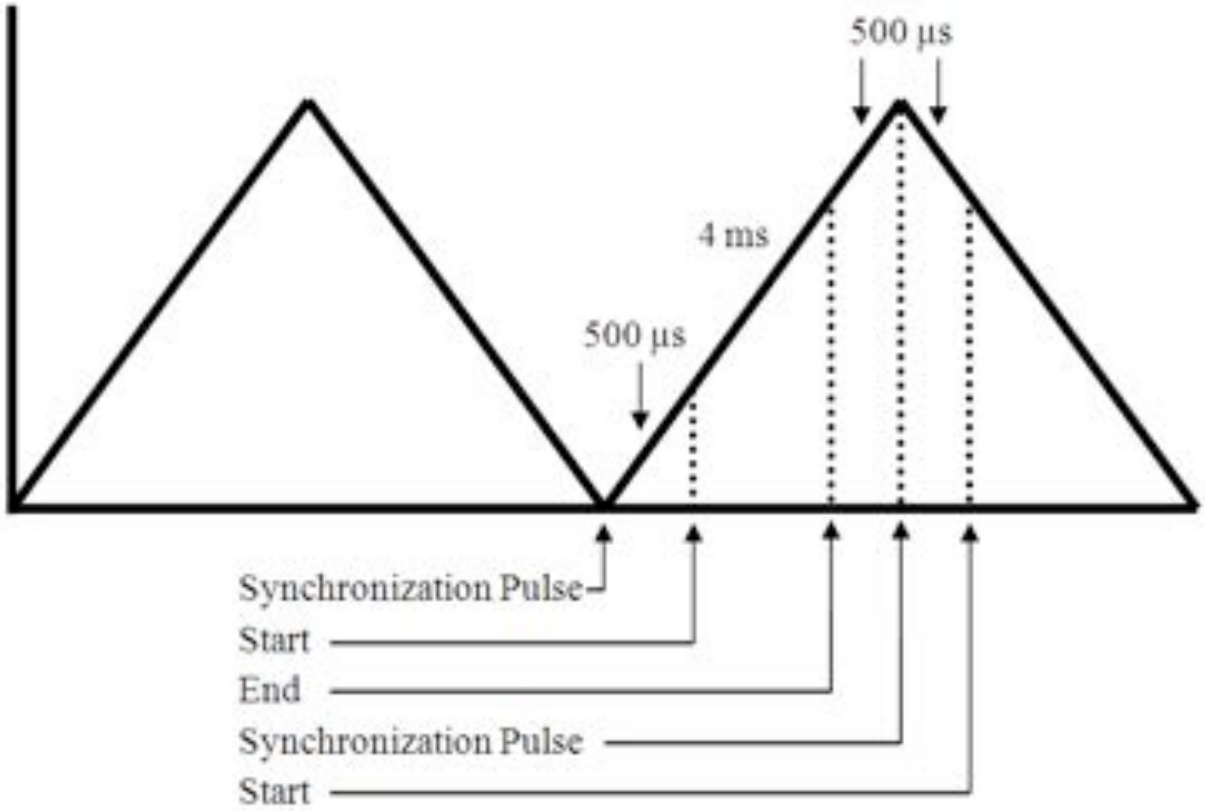
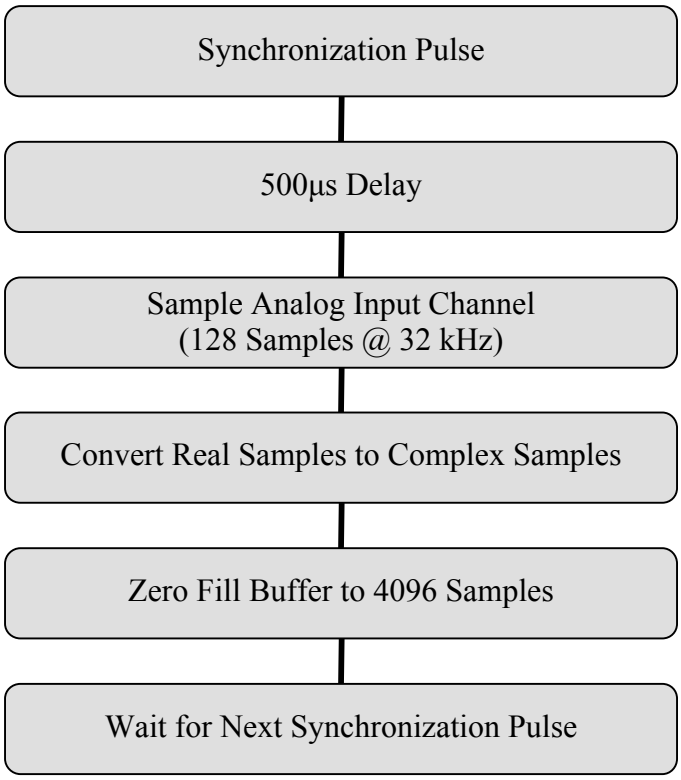


Figure 10 – Digital Signal Processor Sample Timing



To eliminate the possibility of measurement errors, a 500µs delay will be added within the DSP firmware between the detection of a synchronization pulse edge and the start of a sampling window.

Figure 11 – Digital Signal Processor Sample Timing Flow Chart



To determine the dominant frequency present in the sampled radar output, the digital signal processor will pass the sample array through a complex FFT algorithm. The number of FFT points required for a desired range resolution of ±0.5 m is determined as follows:

$$\text{Frequency Resolution} = \frac{\text{Sampling Frequency}}{\text{FFT Points}}$$

$$\text{Range Resolution} = \frac{c}{2} \cdot \frac{T_m}{2} \cdot \frac{\text{Frequency Resolution}}{\text{Bandwidth}}$$

Combining the two formulas together and substituting known values for the sampling frequency, propagation speed, sweep period, and bandwidth, the formula for range resolution can be simplified as follows:

$$\text{Range Resolution} = \frac{300}{\text{FFT Points}}$$

Table 2 – Frequency and Range Resolution as a function of FFT Points

FFT Points	Frequency Resolution (Hz)	Range Resolution (m)
256	125 Hz	1.17 m
512	62.5 Hz	0.59 m
1024	31.25 Hz	0.29 m

Therefore, to achieve the desired range resolution of ±0.50 m, a 1024 point FFT must be performed on the sampled input.

While Microchip Technology provides a complex FFT algorithm as part of their DSP Library, complex FFT coefficients, also known as twiddle factors, are only provided for 64, 128, and 512 point FFT function calls. The algorithm itself, however, is capable of performing a 1024 point FFT calculation.

The only dsPIC33FJ256GP710 specific firmware that is complete is the 1024 point complex FFT coefficient table. This look-up table resides in program memory and will be called by the complex FFT algorithm.

9.0 DOCUMENTS REFERENCED

[1] J. Walz and E. Singh, "Concept Proposal for Automotive Collision Mitigation System", *ICIS*, TP-C1 REV A, 2008.

[2] Industry Canada, "Low-power Licence-exempt Radiocommunication Devices (All Frequency Bands): Category I Equipment," *Industry Canada*, RSS-210 Issue 7, 2007. [Online]. Available: www.ic.gc.ca/epic/site/smt-gst.nsf/vwapj/rss210e.pdf/$FILE/rss210e.pdf [Accessed: Mar. 22, 2008]

[3] Ministry of Transport, "Motor Vehicle Safety Act," January 2008, http://www.tc.gc.ca/acts-regulations/GENERAL/m/mvsa/menu.htm [Accessed: Mar. 26, 2008]

[4] USB Implementers Forum Inc., "Universal Serial Bus Specification," USB Implementers Forum Inc., Revision 2.0, Apr. 2000. [Online]. Available: http://www.usb.org/developers/docs/usb_20_040908.zip [Accessed: May 23, 2008]

[5] International Standards Organization, “Intelligent Transport Systems – Forward Vehicle Collision Warning Systems – Performance and Test Procedures,” *International Standards Organization*, ISO 15623:2002, 2002. [Online]. Available: http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=27835 [Accessed: Jan. 24, 2008]

[6] Society of Automotive Engineers, " Human Factors in Forward Collision Warning Systems: Operating Characteristics and User Interface Requirements," *SAE Standards*, J2400, 2003. [Online]. Available: http://www.sae.org/technical/standards/J2400_200308 [Accessed: Jan. 24, 2008]

10.0 APPENDICIES

10.1 APPENDIX 1 – Hardware Schematics

10.2 APPENDIX 2 – PC Software Source Code

10.3 APPENDIX 3 – PC Software Block Diagram

10.4 APPENDIX 4 – PC Software Flow Chart

10.5 APPENDIX 5 – USB Transceiver Source Code

10.6 APPENDIX 6 – USB VID and PID Sub-Licence